# Wide-Bandwidth *Ku*-Band Monolithic Analog Frequency Divider

S. Desgrez, M. Gayral, O. Llopis, J.-C. Cayrou, J.-L. Cazaux, and J.-F. Sautereau

***Abstract*—A new analog frequency divider configuration using a resistive field-effect transistor (FET) mixer with a series feedback is proposed. With this configuration, a large synchronization bandwidth of almost 30% has been achieved using an original CAD technique. This bandwidth has been effectively measured on a *Ku*-band monolithic microwave integrated circuit (MMIC) circuit together with an ultra-low power consumption. Moreover, the processed circuit using a standard 0.2-$\mu$m PHEMT technology (Philips-PML) is very compact (1.5 mm$^2$).**

***Index Terms*— Analog frequency dividers, MMIC, nonlinear circuits, nonlinear modeling.**

## I. Introduction

THE development of space telecommunication equipment requires the design of sophisticated frequency synthesizers involving many frequency dividers. Thus, the circuits designed for these specific applications must fit various requirements such as a wide frequency range (in our case 12.5–14.5 GHz), a low power consumption, and the ability to be integrated as a module in a larger system.

Analog regenerative frequency dividers are a good choice to simultaneously reach very high operating frequencies, low phase noise, and low power consumption. However, their drawback is the synchronization bandwidth, which is generally restricted to less than 20% [1]–[5].

On the other hand, parametric frequency dividers [6]–[8] allow larger synchronization bandwidth but need much more input power and achieve lower conversion gain. Moreover, parametric division remains a somewhat uncommon process in which a subharmonic oscillation is generated from a passive nonlinear element. It is now well known by experimentalists but has been seldom simulated rigorously.

Our aim has been to define a general simulation technique using a commercial CAD software in order to be able to study and design both types of dividers. In our humble opinion, the dividers' main problem comes from the synchronization bandwidth, because it is only fixed by the divider whereas other parameters can be compensated by external elements. We have therefore investigated new designs in order to improve synchronization bandwidth. An original topology, based on an intermediate approach between a regenerative frequency divider and a parametric one, is proposed in this letter.

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## II. Topology

The resistive field-effect transistor (or cold FET) mixer has been used together with a series feedback and two matching networks as depicted in Fig. 1. It is worth noting that the series feedback allows a low $Q$ factor subharmonic oscillator configuration.

Furthermore, the mixing process in the cold FET is intrinsically a wide-band process. The subharmonic oscillator is self biased by the input signal, in the absence of which, no oscillation can occur.

## III. Design

Time-based simulation is the more natural solution to study analog frequency dividers because it allows direct analyses. But it does not match all requirements for microwave-integrated circuits design. Monolithic microwave integrated circuit (MMIC) designers are much more familiar with harmonic balance technique. But this technique is unable to spontaneously generate the subharmonic frequency which appears in frequency division. Thus, an original approach [3] has been used in which the subharmonic frequency can be imposed by an external generator.

It is based on the assumption that a closed-loop circuit can be represented by an infinite chain of loop elements. Thus, the circuit is no more analyzed as an oscillator but as an amplifier, and this simplifies considerably the analysis. However, it has to be pointed out that this method works only if the amplifying element is unilateral. To satisfy this last requirement, it is necessary to separate the intrinsic transistor effect from the parasitic feedback effect in the FET model. The element chain can then be analyzed with a harmonic balance software. Of course, only a finite number of cells are involved for this analysis (eight cells are generally sufficient to achieve almost all convergence processes).

The main drawback of this technique is a bifurcation-like phenomenon that often appears at high gain compression and/or at locking bandwidth edges. It consists of two (or more) different solutions appearing alternatively in the cascaded cells. We have observed such phenomenon during the study of classical frequency divider topologies. However, no such

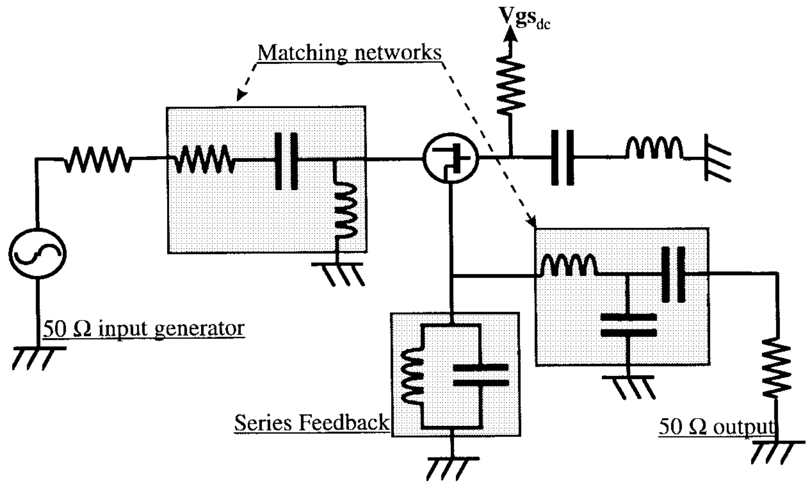


Fig. 1. Topology of the frequency divider.

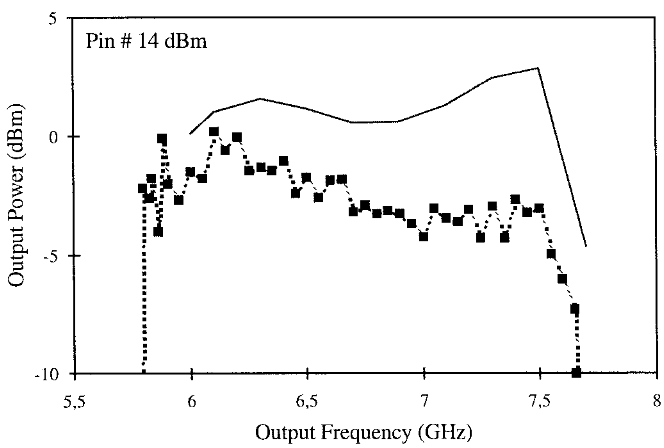


Fig. 2. Measured (squares) and simulated (solid line) locking frequency ranges. Pin #14 dBm, $V_{gs_{\mathrm{dc}}} = -0.65$ V.

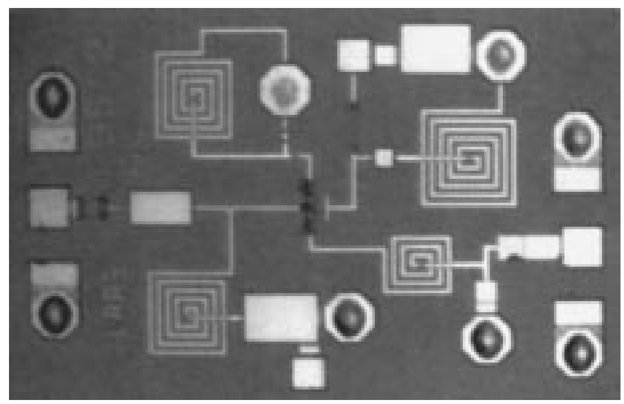

Fig. 3. Photograph of the frequency divider chip.

effects appeared during the cold FET divider design because of lower compression levels.

We have therefore been able to optimize our circuits, particularly the series feedback and the matching networks, in order to increase the frequency synchronization bandwidth.

This theoretical work has resulted in the fabrication of a *Ku*-band frequency divider by two using the models provided by Phillips PML foundry (process D02AH). The FET, or more precisely the PHEMT, is modeled using an equivalent circuit including five nonlinear elements described by polynomial/exponential expressions: the drain–source current, the gate–source capacitance and current, and the gate–drain capacitance and current. The divider-simulated output power versus frequency response is represented in Fig. 2, showing a locking frequency range of about 1.8 GHz.

## IV. Experimental Results

The processed circuit using a standard 0.2-$\mu$m PHEMT technology (Philips-PML) is very compact (1.5 mm$^2$). The photograph of the MMIC is shown in Fig. 3.

A wide frequency bandwidth of about 30% has been experimentally achieved (Fig. 2), thus confirming our expectations. The conversion losses are in the range of 15 dB but can be improved to 12 dB using an external tuner on the output. However losses can be easily reduced adding a cascaded amplifier on the output while the overall dc consumption remains low due to basically zero dc power consumption of the cold FET divider.

The 30% bandwidth corresponds to a serious improvement compared to any type of MMIC analog frequency dividers [3], [5], [8]. Only some varactor-based double-balanced parametric frequency dividers feature better performance with respect to this parameter [6], but higher input power levels are required. In our design, 8 dBm at the input are sufficient to reach almost the maximum frequency bandwidth as depicted in Fig. 4.

No phase noise has been found to be added to a 12.4-GHz source at the input of this circuit. The phase noise of the source was simply divided by 2 from $-117$ dBc/Hz at the input to $-123$ dBc/Hz at the 6.2-GHz output for a 100-kHz frequency offset. A more sophisticated measurement technique involving two identical dividers will soon be used to evaluate more precisely the divider residual phase noise.

## V. Conclusion

A *Ku*-band monolithic analog frequency divider has been successfully modeled, designed, and tested. It involves a single

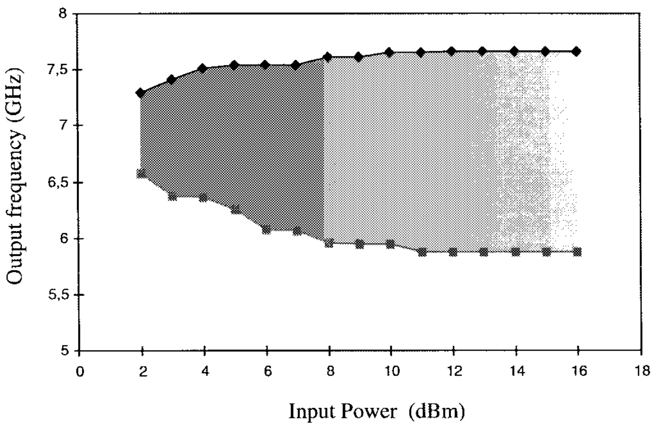


Fig. 4. Measured output frequency range versus input power.

resistive FET. The observed bandwidth outperforms previously reported results for MMIC analog frequency dividers. This circuit can be included in a larger system or cascaded with amplifiers or other dividers to provide a dividing chain featuring a higher division rate. Furthermore, this study can be used to achieve frequency division in the millimeter-wave band very easily.

## ACKNOWLEDGMENT

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## REFERENCES

[1] C. Rausher, “Regenerative frequency division with a GaAs FET,” *IEEE Trans. Microwave Theory Tech.*, vol. 32, pp. 1461–1468, Nov. 1984.

[2] H. Amine, O. Llopis, M. Gayral, J. Graffeuil, and J-F. Sautereau, “New approach to GaAs MESFET analog frequency dividers with low threshold input power and high conversion gain,” *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2345–2351, Dec. 1992.

[3] J.-C. Sarkissian, M. Camiade, P. Savary, A. Suarez, R. Quéré and J. Obregon, “A 60 GHz HEMT MMIC analog frequency divider by two,” *IEEE J. Solid-State Circuits*, vol. 30, pp. 1062–1067, Oct. 1995.

[4] I. Angelov and H. Zirath, “48/24 GHz and 20/10 GHz regenerative frequency dividers,” in *1996 IEEE MTT-S Dig.*, pp. 971–974.

[5] E. Bourdel, B. Delacressonniere, J.-L. Gautier, C. Josse, and P. Pouvil, “Microwave monolithic analogue frequency divider with GaAs HEMT,” *Microwave Opt. Tech. Lett.*, vol. 5, pp. 721–722, Dec. 1992.

[6] R. G. Harrison and W. D. Cornish, “Varactor frequency halvers with enhanced bandwidth and dynamic range,” in *1986 IEEE MTT-S Dig.*, pp. 305–308.

[7] G. R. Sloan, “The modeling, analysis, and design of filter-based parametric frequency dividers,” *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 224–288, Feb. 1993.

[8] S. P. Stapleton, M. G. Stubbs, and J. S. Wight, “GaAs Monolithic analogue frequency halver,” *Electron. Lett.*, vol. 22, pp. 773–774, July 1986.